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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/657,470	09/08/2003	Naoto Hirota	KANEKO.008AUS	9817
	7590 09/26/200 J & ASSOCIATES	EXAMINER		
114 PACIFICA			CALEY, MICHAEL H	
SUITE 310 Irvine, CA 926	18		ART UNIT	PAPER NUMBER
			2871	
			MAIL DATE	DELIVERY MODE
			09/26/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

		Application No.	Applicant(s)		
		10/657,470	HIROTA, NAOTO		
	Office Action Summary	Examiner	Art Unit		
		MICHAEL H. CALEY	2871		
D : 16	The MAILING DATE of this communication ar	ppears on the cover sheet wi	th the correspondence address		
	or Reply				
WHI0 - Exte after - If No - Failt Any	HORTENED STATUTORY PERIOD FOR REPLICHEVER IS LONGER, FROM THE MAILING IDENTION OF THE MAILING OF THE MAIL	DATE OF THIS COMMUNIC 1.136(a). In no event, however, may a red d will apply and will expire SIX (6) MON tite, cause the application to become AB	CATION. reply be timely filed ITHS from the mailing date of this communication. BANDONED (35 U.S.C. § 133).		
Status					
1)🛛	Responsive to communication(s) filed on 25.	<u>June 2008</u> .			
2a)⊠	☐ This action is FINAL . 2b) This action is non-final.				
3)□	Since this application is in condition for allowa	ance except for formal matte	ers, prosecution as to the merits is		
	closed in accordance with the practice under	Ex parte Quayle, 1935 C.D	. 11, 453 O.G. 213.		
Disposit	tion of Claims				
4)⊠	Claim(s) <u>1,3,4,6,7,9,10,12,13,15,16 and 18-5</u>	54 is/are pending in the appl	ication.		
<i>,</i> —	4a) Of the above claim(s) <u>9,10,12,13,15,16 ar</u>				
5)	Claim(s) is/are allowed.				
6)🖂	Claim(s) <u>1,3,4,6,7,53 and 54</u> is/are rejected.				
	Claim(s) is/are objected to.				
8)□	Claim(s) are subject to restriction and/	or election requirement.			
Applicat	tion Papers				
9)□	The specification is objected to by the Examin	ner.			
10)🛛	The drawing(s) filed on <u>08 September 2003</u> is	s/are: a)⊠ accepted or b)□	objected to by the Examiner.		
	Applicant may not request that any objection to the	e drawing(s) be held in abeyan	ce. See 37 CFR 1.85(a).		
_	Replacement drawing sheet(s) including the corre-		• • •		
11)	The oath or declaration is objected to by the E	Examiner. Note the attached	d Office Action or form PTO-152.		
Priority	under 35 U.S.C. § 119				
12)🔯	Acknowledgment is made of a claim for foreig	n priority under 35 U.S.C. §	119(a)-(d) or (f).		
)⊠ All b)□ Some * c)□ None of:				
	1. Certified copies of the priority documer	nts have been received.			
	2. Certified copies of the priority documer	nts have been received in A	pplication No		
	3. Copies of the certified copies of the price	•	received in this National Stage		
	application from the International Burea				
^;	See the attached detailed Office action for a lis	st of the certified copies not	received.		
Attachmer	nt(s)				
	ce of References Cited (PTO-892)		Summary (PTO-413)		
3) 🔲 Infor	ce of Draftsperson's Patent Drawing Review (PTO-948) rmation Disclosure Statement(s) (PTO/SB/08) er No(s)/Mail Date	<u> </u>	s)/Mail Date nformal Patent Application		

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DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al. (U.S. Patent No. 6,407,791 "Suzuki").

Regarding claim 1, Suzuki discloses a color active matrix type vertically aligned mode liquid crystal display comprising on a substrate:

a scan signal wiring (Figure 8 element 55);

a video signal wiring (Figure 8 element 56);

a thin film transistor (54) which is formed at an intersection of the scan signal wiring and the video signal wiring;

a transparent pixel electrode (Figure 8 element 71; Column 10 line 52) connected to the thin film transistor (Figure 14) element in which two or more long and slender slits are formed (Figure 8 element 74);

an active matrix substrate (Figure 9 element 11) having a liquid crystal alignment direction control electrode (Figure 8 element 73) in a lower layer of the slits of the transparent pixel electrode currently formed via an insulator film (Figure 9 element 62); a substrate (Figure 9 element 12) facing the active matrix substrate; and

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an anisotropic liquid crystal layer (Figure 9 element 20) having a negative dielectric constant (Column 5 lines 50-53);

wherein in order to impress a voltage to liquid crystal molecules vertically aligned (Figure 9 element 20) between the active matrix substrate and the other substrate, and to make the liquid crystal molecules tilt in different two directions (Figure 9 element 20), two kinds of following electrode structures are formed in one pixel of the active matrix substrate:

- (i) an electrode structure in which a transparent flat common electrode (Figure 9 element 81) is used on the other substrate side, and for the transparent pixel electrodes facing the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed (Figure 8 element 74);
- (ii) an electrode structure in which a transparent flat common electrode is used in the other substrate side, and for the transparent pixel electrode facing the transparent flat common electrode in the active matrix substrate side, patterns having a shape of a long and slender slit are formed, and a liquid crystal alignment direction control electrode having almost the same shape as a shape of the slits and a larger dimension than a dimension of the slits is formed in a lower layer of the slits (Figures 8 and 9 element 73) via the insulator film (Figure 9 element 62) where the transparent pixel electrode and the liquid crystal alignment direction control electrode in each pixel of the active matrix substrate are driven separately from one another (Column 11 lines 9-23).

Suzuki fails to disclose the other substrate facing the active matrix substrate as a color filter substrate. In a separate embodiment, however, Suzuki teaches that the substrate facing the active matrix substrate may have a color filter (Column 12 lines 12-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the substrate other than the active matrix substrate as a color filter substrate.

One would have been motivated to form the substrate as a color filter substrate to benefit from color display.

Regarding claim 7, Suzuki discloses adjacent transparent pixel electrodes in a direction of the scan signal wiring are connected to a thin film transistor component controlled by mutually different scan signal wirings (Figure 8).

Claims 3, 4, 6, 53, and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki in view of Watanabe (U.S. Patent No. 6,665,023).

Regarding claim 3, Suzuki discloses the display such that:

when a potential of the transparent pixel electrode separated for every pixel of the active matrix substrate side is lower than a potential of the facing flat common electrode on the color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set lower than a potential of the transparent pixel electrode (Column 11 lines 1-8, Column 11 lines 24-31); and

when a potential of the transparent pixel electrode separated for every pixel of the active matrix substrate side is higher than a potential of the facing flat common electrode on the color filter substrate side, a potential of the liquid crystal alignment direction control electrode currently placed in a lower layer of the slit of the transparent pixel electrode is set higher than a potential of the transparent pixel electrode (Column 11 lines 1-8, Column 11 lines 24-31).

Watanabe fails to disclose the polarities of the potential of the transparent pixel electrode, and the potential of the liquid crystal alignment control electrode as reversed to a polarity of the potential of the flat common electrode in the color filter substrate side every vertical scanning period. Watanabe, however, teaches such a reversal of polarity for every vertical scanning period as a means of reducing flicker (Column 3 lines 39-42, Column 4 lines 45-62).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to drive the display disclosed by Suzuki by reversing the polarity in every vertical scanning period. One would have been motivated to drive the display as proposed to reduce display flicker (Column 3 lines 39-42, Column 4 lines 45-62).

Regarding claims 4, 6, 53, and 54, Suzuki as modified by Watanabe further discloses two rows of liquid crystal alignment direction control electrodes that are mutually separated and set at potentials different from each other and as mutually exchanged in every fixed pixel cycle, due to polarity inversion between pixels.

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Applicant's arguments filed 6/25/08 have been fully considered but they are not persuasive.

Applicant has amended claims 1, 4, and 7 to feature the transparent pixel electrode and the liquid crystal alignment direction control electrode in each pixel of the active matrix substrate as driven separately from one another. Applicant argues that such a feature distinguishes the claimed invention from the disclosure of Suzuki.

The examiner disagrees and maintains the rejection. Suzuki discloses the transparent pixel electrode (71) voltage as determined by the common capacitor line and the ratio of capacitance among coupling capacitors (Column 11 lines 14-19). Suzuki discloses the alignment direction control electrode (73) voltage, however, as fed through the TFT from the video signal line (Column 11 lines 9-13). Since the pixel electrode voltage is partially determined by the voltage of the common capacitor line, the electrodes are considered to be driven separately from one another.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL H. CALEY whose telephone number is (571)272-2286. The examiner can normally be reached on M-F 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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/Michael H. Caley/ Primary Examiner, Art Unit 2871